impurity doped regions;

a storage electrode formed in said upper part of said insulating laminate and electrically connected to said first conductor;

a capacitor insulating film formed on said storage electrode;

an opposing electrode covering said capacitor insulating film and having an extension formed over said lower part of said insulator laminate;

a second contact hole, formed through said upper part of said insulating laminate, penetrating said extension of said opposing electrode;

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at its side wall exposed in said second contact hole;

a third contact hole, formed in said insulating laminate, exposing a third conductor and being deeper than said second contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to a surface of said third conductor.

39. A semiconductor memory device according to claim 38, wherein said third conductor is disposed in said lower part of said insulating laminate.

40. A semiconductor memory device according to claim 38, wherein said third conductor is an impurity doped region formed in said semiconductor substrate.

41. A semiconductor memory device according to claim 38, wherein said lower part of said insulator laminate includes a nitride film at an uppermost level.

42. A semiconductor memory device according to claim 38, wherein said storage electrode is a cylinder type storage electrode.

43. A semiconductor memory device according to claim 38, wherein said opposing electrode is composed of a polysilicon and said third conductor is a metal silicide.

44. A semiconductor memory device according to claim 38, wherein said upper part of said insulator laminate has a planarized upper surface.

45. A semiconductor memory device according to claim 39, wherein a first nitride film is disposed between said opposing electrode and said semiconductor substrate, and said third conductor is covered with a second nitride film.

46. A semiconductor memory device according to claim 38 further comprising:

a fourth contact hole, formed through said insulator laminate, exposing said semiconductor substrate and being deeper than said third contact hole; and

a fifth conductor filled in said fourth contact hole and electrically connected to said semiconductor substrate,

wherein said third conductor is disposed in said lower part of said insulator laminate.

47. A semiconductor memory device comprising:

a first insulator formed over a semiconductor substrate;

a memory cell transistor;

a memory cell capacitor, formed over said first insulator, having a first electrode electrically

connected to said memory cell transistor, a capacitor insulating film and a second electrode;

a second insulator covering said memory cell transistor and said memory cell capacitor;

a contact hole formed through said second insulator and said second electrode; and

a conductor, filled in said contact hole, for applying a predetermined potential to said second electrode, wherein said conductor is electrically connected to said second electrode at its side wall exposed in said contact hole.

48. A semiconductor memory device according to claim 47, wherein said first electrode is a cylinder type storage electrode having a bottom portion electrically connected to said memory cell transistor and a cylindrical portion extending upwardly.

49. A semiconductor memory device according to claim 48, wherein a height of said cylinder type storage electrode is larger than its width.

50. A semiconductor memory device comprising:

a first insulator formed over a semiconductor substrate;

a wiring disposed in said first insulator;

a memory cell transistor;

a memory cell capacitor, formed over said first insulator, having a first electrode electrically connected to said memory cell transistor, a capacitor insulating film and a second electrode;

a second insulator covering said memory cell transistor and said memory cell capacitor;

a first contact hole formed through said second insulator and said second electrode;

a first conductor, filled in said first contact hole, for applying a predetermined potential to said second electrode, wherein said first conductor is electrically connected to said second electrode at its side wall exposed in said contact hole;

a second contact hole exposing a surface of said wiring through said first and second insulators; and

a second conductor filled in said second contact hole, wherein said second conductor is electrically connected to said wiring at said surface.

51. A semiconductor memory device according to claim 50, wherein said second electrode is composed of a different conductive material from a conductive material of said wiring.

52. A semiconductor memory device according to claim 50, wherein said second electrode is composed of a polysilicon, and said wiring is a metal silicide.

53. A semiconductor memory device according to claim 50, further comprising a third insulator, disposed between said second electrode and said semiconductor substrate, having etching characteristics different from that of said second insulator.

54. A semiconductor memory device according to claim 53, wherein said third insulator is composed of a nitride film.

55. A semiconductor memory device according to claim 50, wherein said wiring is covered with a nitride film.

56. A semiconductor memory device according to claim 50, wherein said first contact hole is located in a memory cell area, said second contact hole is located in a peripheral circuit area.

57. A semiconductor memory device according to claim 50, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.

58. A semiconductor memory device comprising:

a first insulator formed over a semiconductor substrate;

a wiring disposed in said first insulator;

an impurity doped region formed in said semiconductor substrate;

a memory cell transistor;

a memory cell capacitor, formed over said first insulator, having a first electrode electrically connected to said memory cell transistor, a capacitor insulating film and a second electrode;

a second insulator covering said memory cell transistor and said memory cell capacitor;

a first contact hole formed through said second insulator and said second electrode;

a first conductor, filled in said first contact hole, for applying a predetermined potential to said second electrode, wherein said first conductor is electrically connected to said second electrode at its side wall exposed in said first contact hole;

a second contact hole exposing a surface of said wiring through said first and second insulators;

a second conductor filled in said second contact hole, wherein said second conductor is electrically connected to said wiring at said surface;

a third contact hole exposing a surface of said impurity doped region through said first and second insulators; and

a third conductor filled in said third contact hole, wherein said third conductor is electrically connected to said impurity doped region at said surface.

59. A semiconductor memory device according to claim 58, wherein said second electrode is composed of a different conductive material from a conductive material of said wiring.

60. A semiconductor memory device according to claim 58, wherein said second electrode is composed of a polysilicon, and said wiring is a metal silicide.

61. A semiconductor memory device according to claim 58, further comprising a third insulator, disposed between said second electrode and said semiconductor substrate, having etching characteristics different from that of said second insulator.

62. A semiconductor memory device according to claim 61, wherein said third insulator is composed of a nitride film.

63. A semiconductor memory device according to claim 58, wherein said wiring is covered with a nitride film.

64. A semiconductor memory device according to claim 58, wherein said first contact hole is located in a memory cell area, and said second and third contact holes are located in a peripheral circuit area.

65. A semiconductor memory device according to claim 58, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.

66. A semiconductor memory device according to claim 58, wherein a third insulator is disposed between said second electrode and said semiconductor substrate, said wiring is covered with a fourth insulator, and said third and fourth insulators have different etching characteristics from that of said second insulator.

67. A semiconductor memory device according to claim 66, wherein said third insulator is composed of a first nitride film, and said fourth insulator is composed of a second nitride film.

68. A semiconductor memory device according to claim 58, wherein said first electrode is a cylinder type storage electrode having a bottom portion electrically connected to said memory cell transistor and a cylindrical portion extending upwardly.

69. A semiconductor memory device according to claim 68, further comprising a third insulator, disposed between said second and first insulators, having an opening, wherein said bottom portion of said cylinder type storage electrode is disposed in said opening and said cylindrical portion is disposed in said second insulator.

70. A semiconductor memory device according to claim 68, wherein said cylinder type storage electrode has a height larger than its width.

71. A semiconductor memory device according to claim 69, wherein said second electrode is extending over said third insulator.

72. A semiconductor memory device according to claim 58, wherein each of said first and second insulators has a planarized surface.

73. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell transistor having a gate electrode and impurity doped regions formed in said semiconductor substrate;

a first insulator formed over said semiconductor substrate covering said memory cell transistor and having a planarized surface;

a first contact hole, formed through said first insulator, exposing one of said impurity doped regions;

a first conductor filled in said first contact hole;

a second insulator, formed over said first insulator, having a planarized surface and an opening exposing said first conductor;

a memory cell capacitor having a cylinder type storage electrode electrically connected to said one of said impurity doped regions via said first conductor, a capacitor insulating film and an opposing electrode,

wherein said cylinder type storage electrode has a lower portion disposed in said opening and an upper portion extending upwardly, said opposing electrode faces said cylinder type storage electrode via said capacitor insulating film and extends over said second insulator;

a third insulator formed over said second insulator, covering said memory cell capacitor and having a planarized surface;

a second contact hole penetrating said third insulator and said opposing electrode disposed over said second insulator,

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at its side wall exposed in said second contact hole;

a third contact hole of which a depth from said planarized surface of said third insulator is larger than a depth of said second contact hole; and

a third conductor having a surface exposed in said third contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to said third conductor at its surface.

74. A semiconductor memory device according to claim 73, wherein said third conductor is disposed in said first insulator.

75. A semiconductor memory device according to claim 73, wherein said third conductor is an impurity doped region formed in said semiconductor substrate.

76. A semiconductor memory device according to claim 73, further comprising a field insulating film between said semiconductor substrate and said first insulator, wherein said third conductor is formed over said field insulating film.

77. A semiconductor memory device according to claim 73, wherein a diameter of said opening of said second insulator is larger than a diameter of said first contact hole.

78. A semiconductor memory device according to claim 73, wherein a height of said cylinder type storage electrode is larger than its width.

79. A semiconductor memory device according to claim 73, wherein said cylinder type storage electrode has an inner wall and an outer wall facing said opposing electrode via a capacitor insulating film.

80. A semiconductor memory device according to claim 73, wherein a fourth insulator is disposed between said second insulator and said opposing electrode, said third conductor is covered with a fifth insulator, and each of said fourth and fifth insulators has different etching characteristics from that of said third insulator.

81. A semiconductor memory device according to claim 73, further comprising wirings, formed over said third insulator and electrically connected to said second and fourth conductors respectively.

82. A semiconductor memory device according to claim 73, further comprising:

a fourth contact hole, formed through said third, second and first insulators, exposing a surface of said semiconductor substrate, and

a fifth conductor filled in said fourth contact hole,

wherein said third conductor is disposed in said first insulator, and a depth of said fourth contact hole is larger than said depth of said third contact hole.

83. A semiconductor memory device according to claim 73, wherein another of said impurity doped regions of said memory cell transistor is electrically connected to a bit line which is composed of a lower conductive layer than said cylinder type storage electrode.

84. A semiconductor memory device according to claim 73, wherein said opposing electrode is composed of a different conductive material from a conductive material of said third conductor.

85. A semiconductor memory device according to claim 73, wherein said opposing electrode is composed of a polysilicon, and said third conductor is a metal silicide.

86. A semiconductor memory device according to claim 73, further comprising a fourth insulator, disposed between said opposing electrode and said second insulator, having etching

characteristics different from that of said third insulator.

87. A semiconductor memory device according to claim 86, wherein said fourth insulator is composed of a nitride film.

88. A semiconductor memory device according to claim 73, wherein said third conductor is covered with a nitride film.

89. A semiconductor memory device according to claim 73, wherein said first and second contact holes are located in a memory cell area, and said third contact hole is located in a peripheral circuit area.

90. A semiconductor memory device according to claim 73, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.

91. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of memory cells each comprising a memory cell transistor having a gate electrode and impurity doped regions formed in said semiconductor substrate and a memory cell capacitor having a cylinder type storage electrode electrically connected to said one of said impurity doped regions, a capacitor insulating film and an opposing electrode ;

a first insulator, formed over said semiconductor substrate, covering said memory cell

transistor and having a planarized surface;

first contact holes, formed through said first insulator, each exposing one of said impurity doped regions of each of said memory cell transistors;

first conductors filled in said first contact holes;

a second insulator, formed over said first insulator, having a planarized surface and openings exposing said each of said first conductors, wherein each said cylinder type storage electrode has a lower portion disposed in said openings and an upper portion extending

upwardly, each said opposing electrode is composed of a common conductive layer facing each said cylinder type storage electrode via said capacitor insulating film and extending over said second insulator;

a third insulator, formed over said second insulator, covering each said memory cell capacitor and having a planarized surface;

a second contact hole penetrating said third insulator and said common conductive layer disposed over said second insulator;

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at its side wall exposed in said second contact hole;

a third contact hole of which a depth from said planarized surface of said third insulator is larger than a depth of said second contact hole; and

a third conductor having a surface exposed in said third contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to said third conductor at its surface.

92. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell transistor having a gate electrode and impurity doped regions formed in said semiconductor substrate;

a first insulator, formed over said semiconductor substrate, covering said memory cell transistor and having a planarized surface;

a first contact hole, formed through said first insulator, exposing one of said impurity doped regions;

a first conductor filled in said first contact hole;

a memory cell capacitor having a cylinder type storage electrode electrically connected to said one of said impurity doped regions via said first conductor, a capacitor insulating film and an opposing electrode,

wherein said cylinder type storage electrode has a lower portion disposed over said first contact hole and an upper portion extending upwardly, said opposing electrode faces said cylinder type storage electrode via said capacitor insulating film and extends over said first insulator;

a second insulator, formed over said first insulator, covering said memory cell capacitor and having a planarized surface;

a second contact hole penetrating said second insulator and said opposing electrode disposed over said first insulator,

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at its side wall exposed in said second contact hole;

a third contact hole of which a depth from said planarized surface of said second insulator is larger than a depth of said second contact hole; and

a third conductor having a surface exposed in said third contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to said third conductor at its surface.

93. A semiconductor memory device according to claim 92, wherein said third conductor is disposed in said first insulator.

94. A semiconductor memory device according to claim 92, wherein said third conductor is an impurity doped region formed in said semiconductor substrate.

95. A semiconductor memory device according to claim 92, further comprising a field insulating film between said semiconductor substrate and said first insulator, wherein said third conductor is formed over said field insulating film.

96. A semiconductor memory device according to claim 92, wherein a height of said cylinder type storage electrode is larger than its width.

97. A semiconductor memory device according to claim 92, wherein said cylinder type storage electrode has an inner wall and an outer wall facing said opposing electrode via a capacitor insulating film.

98. A semiconductor memory device according to claim 92, wherein said second insulator has different etching characteristics from that of said opposing electrode.

99. A semiconductor memory device according to claim 92, further comprising wirings, formed over said second insulator, electrically connected to said second and fourth conductors respectively.

100. A semiconductor memory device according to claim 92, further comprising:

a fourth contact hole, formed through said second and first insulators, exposing a surface of said semiconductor substrate, and

a fifth conductor filled in said fourth contact hole,

wherein said third conductor is disposed in said first insulator, and a depth of said fourth contact hole is larger than said depth of said third contact hole.

101. A semiconductor memory device according to claim 92, wherein another of said impurity doped regions of said memory cell transistor is electrically connected to a bit line which is composed of lower conductive layer than said cylinder type storage electrode.

102. A semiconductor memory device according to claim 92, wherein said opposing electrode is composed of a different conductive material from a conductive material of said third conductor.

103. A semiconductor memory device according to claim 92, wherein said opposing electrode is composed of a polysilicon, and said third conductor is a metal silicide.

104. A semiconductor memory device according to claim 92, further comprising a third insulator, disposed between said opposing electrode and said semiconductor substrate, having etching characteristics different from that of said second insulator.

105. A semiconductor memory device according to claim 92, wherein said third insulator is composed of a nitride film.

106. A semiconductor memory device according to claim 92, wherein said third conductor is covered with a nitride film.

107. A semiconductor memory device according to claim 92, wherein said first and second contact holes are located in a memory cell area, and said third contact hole is located in a peripheral circuit area.

108. A semiconductor memory device according to claim 92, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.